

PCIe® Electrical Basics

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AMD

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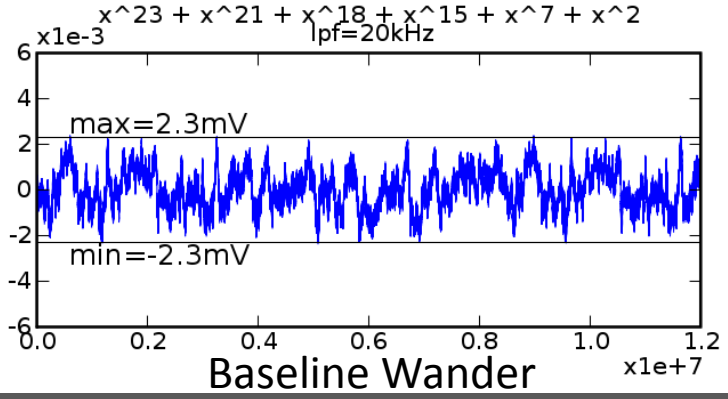
Topics

- **PCI Express® Overview**
- **Target Channels for the Specification**
- **Transmitter**
- **Receiver**
- **Seasim**

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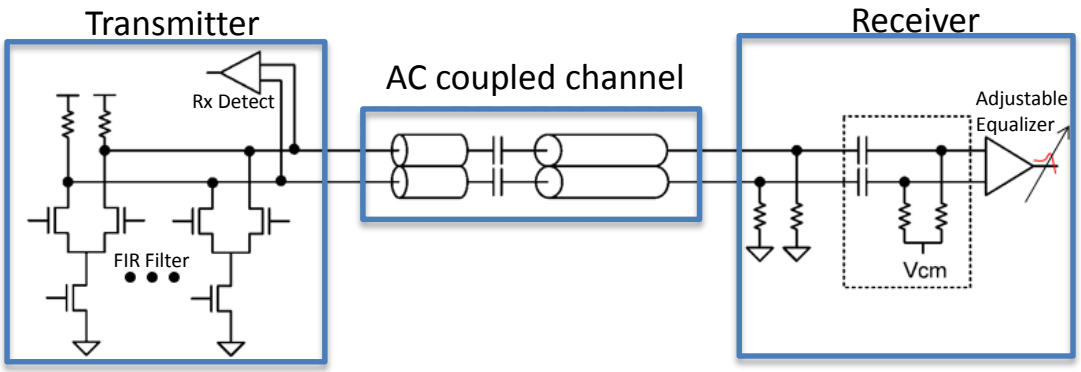
Electrical Overview

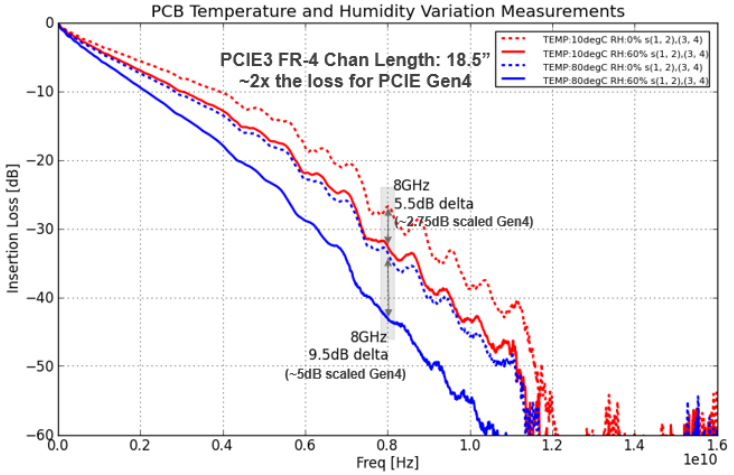
- **Data rates 2.5GT/s, 5GT/s, 8GT/s, 16GT/s**
 - 10^{-12} bit error ratio for all link widths: 1, 2, 4, 8, 16, 32 lanes
 - Receiver equalization included for PCIe 3.0 rate and beyond
- **Channel specification**
 - Card Electromechanical (CEM) spec defines measurements
- **2.5 and 5GT/s scrambled + 8b10b**
- **8GT/s, 16GT/s scrambled + 128/130**
 - Mitigates baseline wander with 20% better efficiency than 8b10b
 - LFSR offsets between adjacent lanes reduces SSN



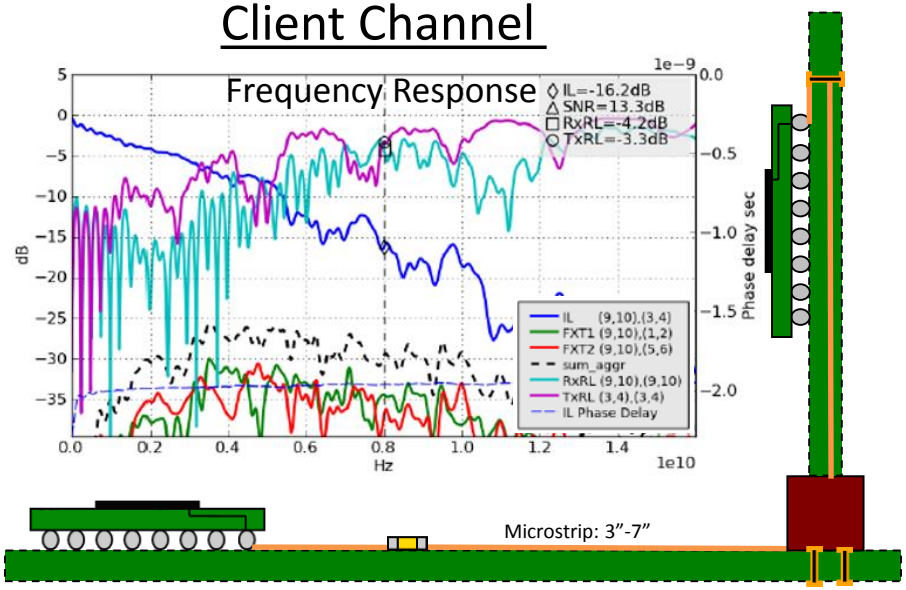
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Transceiver and Channel

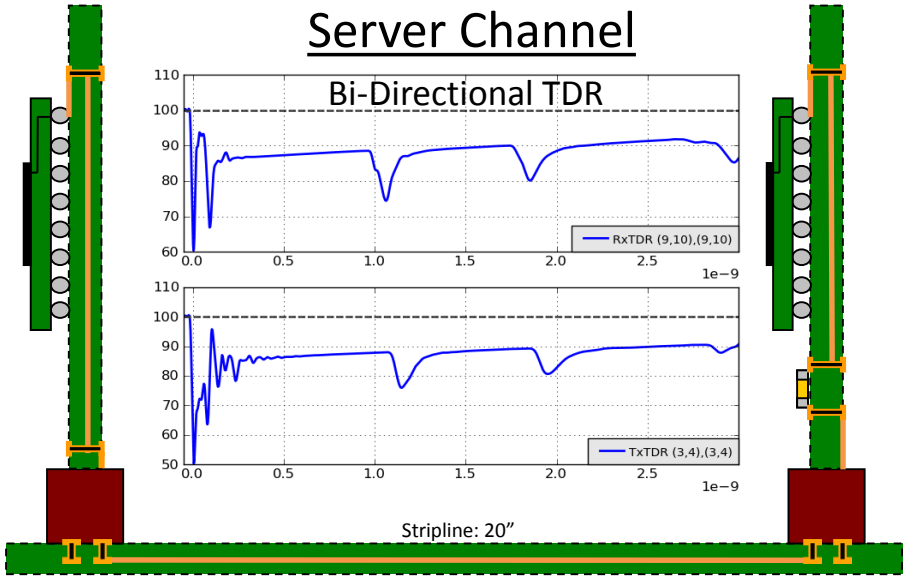




Client Channel



Server Channel



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Transmitter

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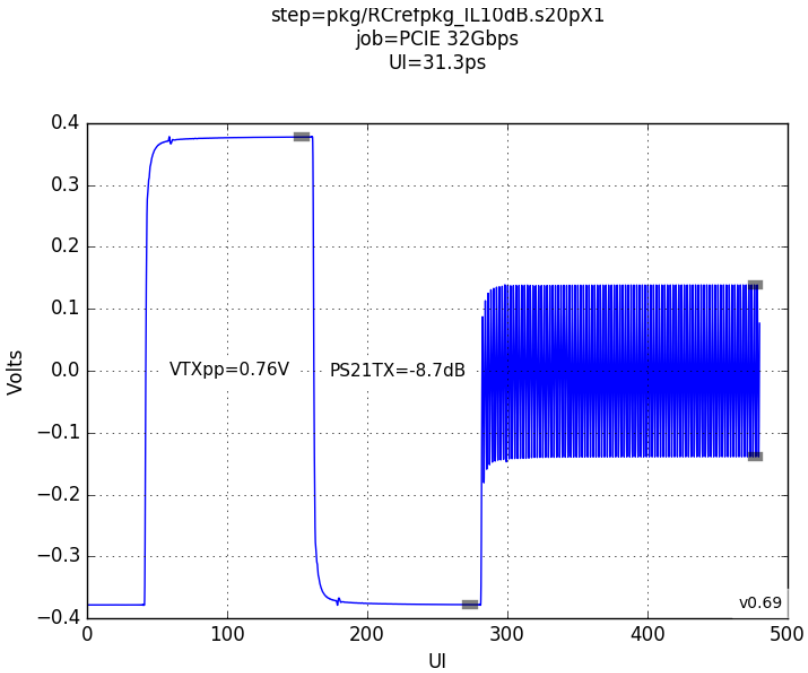
Transmitter Reference Plane

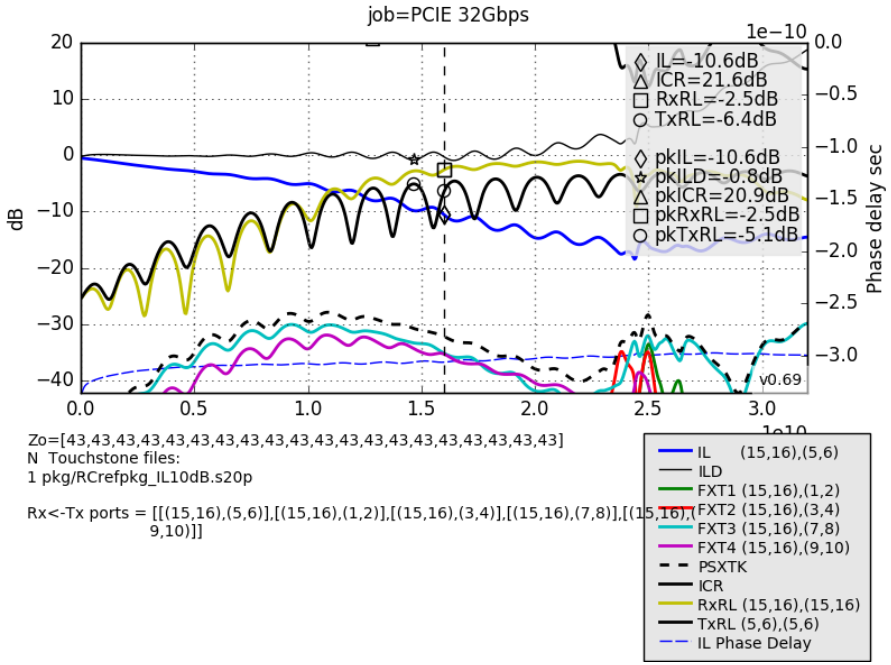
- **Reference plane is DUT pin**
 - Most convenient manufacturing boundary
- **For 2.5 and 5GT/s**
 - Package losses are part of Tx performance
- **Package route and package pin interactions are more significant for higher data rates**
 - Makes fixture de-embedding inaccurate
 - Tx EQ and jitter measurements inaccurate
- **Use data-dependent jitter separation**
 - Effectively measure Tx jitter at die pad
 - Use LF measurement technique for presets at pin

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Transmitter Specification

- **Preset definition**
 - Retain P0-P10 with same definition for 8GT/s & 16GT/s
- **Package loss (ps21TX)**
 - Informative for root complex devices, normative for AIC devices





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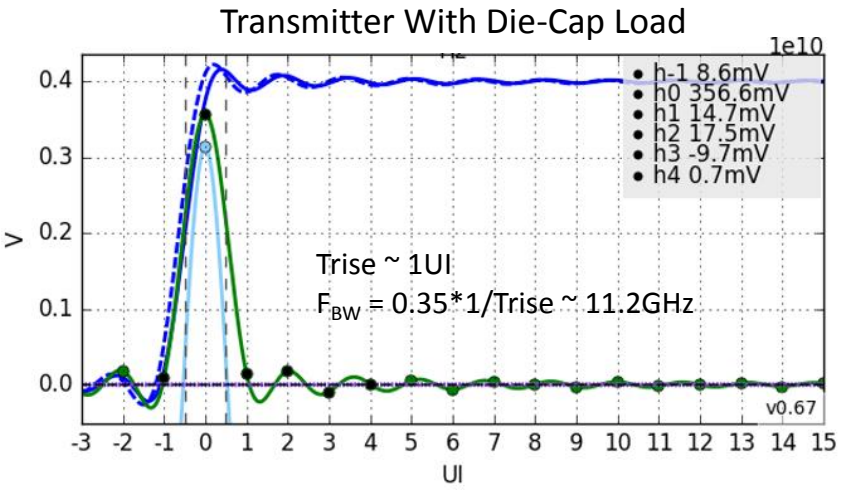
Transmitter

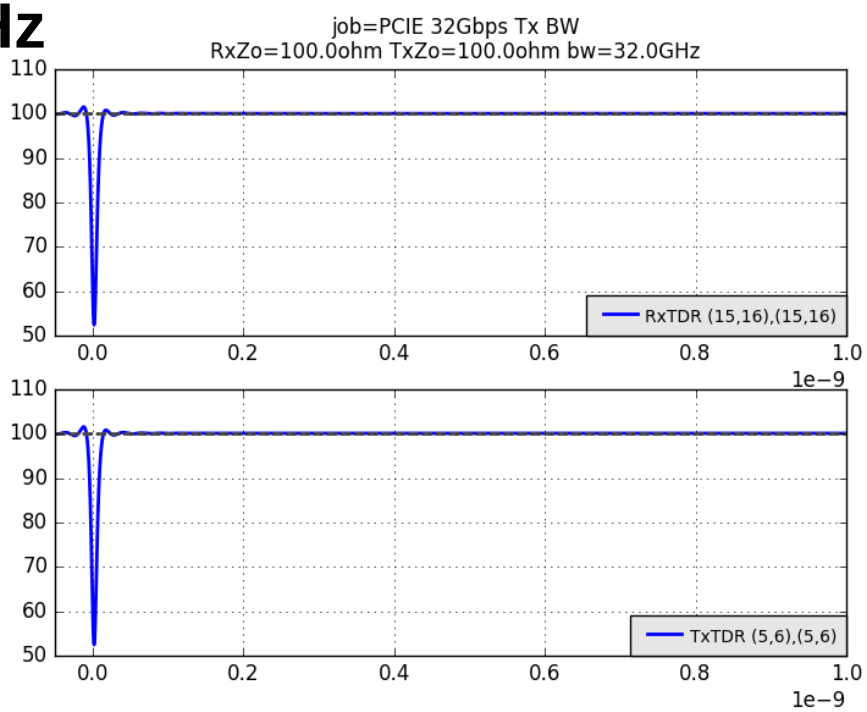
- **Differential ~100ohm transmitter**
 - FS: 800-1200mV, HS: 400-800mV
 - 0.75UI eye opening
- **2.5/5GT/s 2-tap EQ**
 - FS: -3.5dB and -6dB, HS: 0dB
- **8GT/s & 16GT/s 3-tap EQ**
 - 10 presets, min boost 8dB, coefficient tuning space
- **AC coupled channel series capacitor**
 - 2.5/5GT/s 75-265nF
 - 2.5/5/8GT/s (Rev 3.0) 176-265nF
- **Return Loss**
 - SDD11 -10dB 2.5GT/s, -8dB 5GT/s, -4dB 8GT/s (differential)
 - SCC11 -6dB, -3dB 8GT/s (common-mode)

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Silicon Bandwidth

- **Transmitter Gaussian bandwidth definition excludes the die load capacitance, final bandwidth is less**
- **Same condition applies to receiver input bandwidth, specified as FP2**
- **Ex: Driver bandwidth 32GHz**





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Tx FIR EQ Definitions

$$V_{TX} = V_{PK} \sum_{n=0}^{k} c_n d_{m-n} \text{ and } \sum_{n=0}^{k} |c_n| = 1$$

V_{TX} is output voltage and V_{PK} the peak voltage

k is number of Tx coefficients

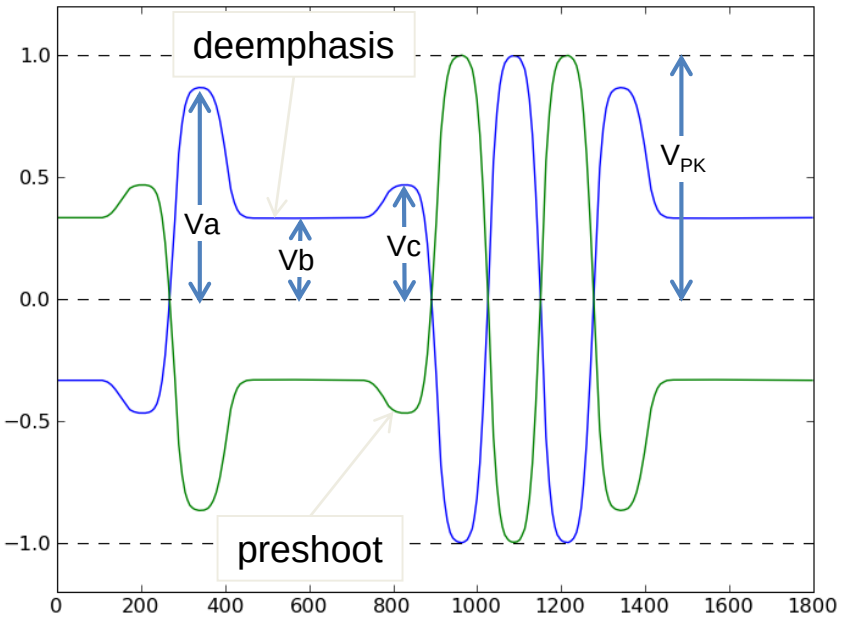
d is vector of +1 and -1 for logic 1 and 0

m is the index into the bit stream

For a 3 tap Gen3 FIR c_1 is positive and

c_0 and c_2 are negative

data is delayed by 1UI



For data stream 00010111

$V_{PK} = 1$ and $t_0 = -c_0; \quad t_1 = c_1; \quad t_2 = -c_2$

$000 \rightarrow +t_0 - t_1 + t_2$

$001 \rightarrow -t_0 - t_1 + t_2$

$011 \rightarrow -t_0 + t_1 + t_2 \rightarrow Va$

$111 \rightarrow -t_0 + t_1 - t_2 \rightarrow Vb$

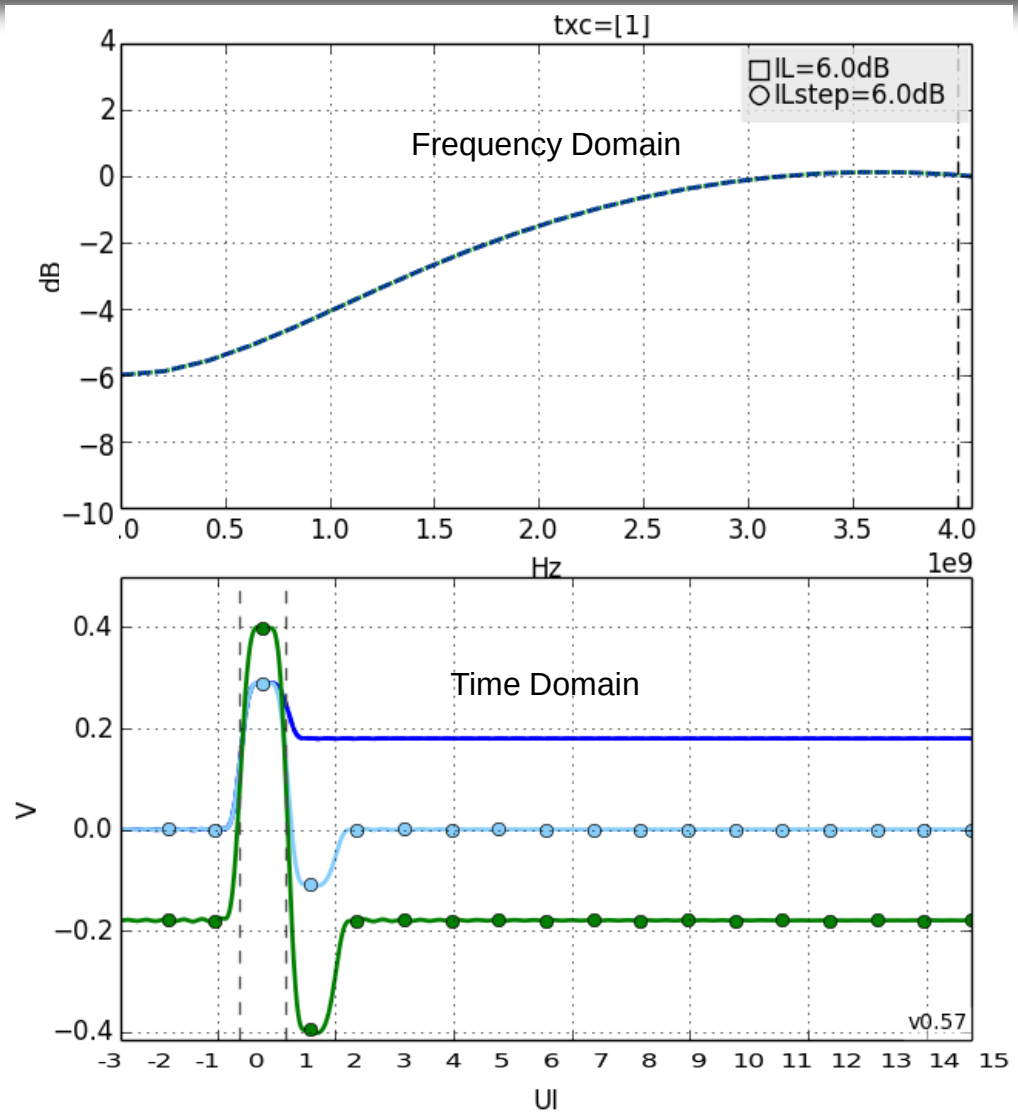
$110 \rightarrow +t_0 + t_1 - t_2 \rightarrow Vc$

$$deemphasis = 20\log_{10}\frac{Vb}{Va}$$

$$preshoot = 20\log_{10}\frac{Vc}{Vb}$$

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Transmit De-Emphasis



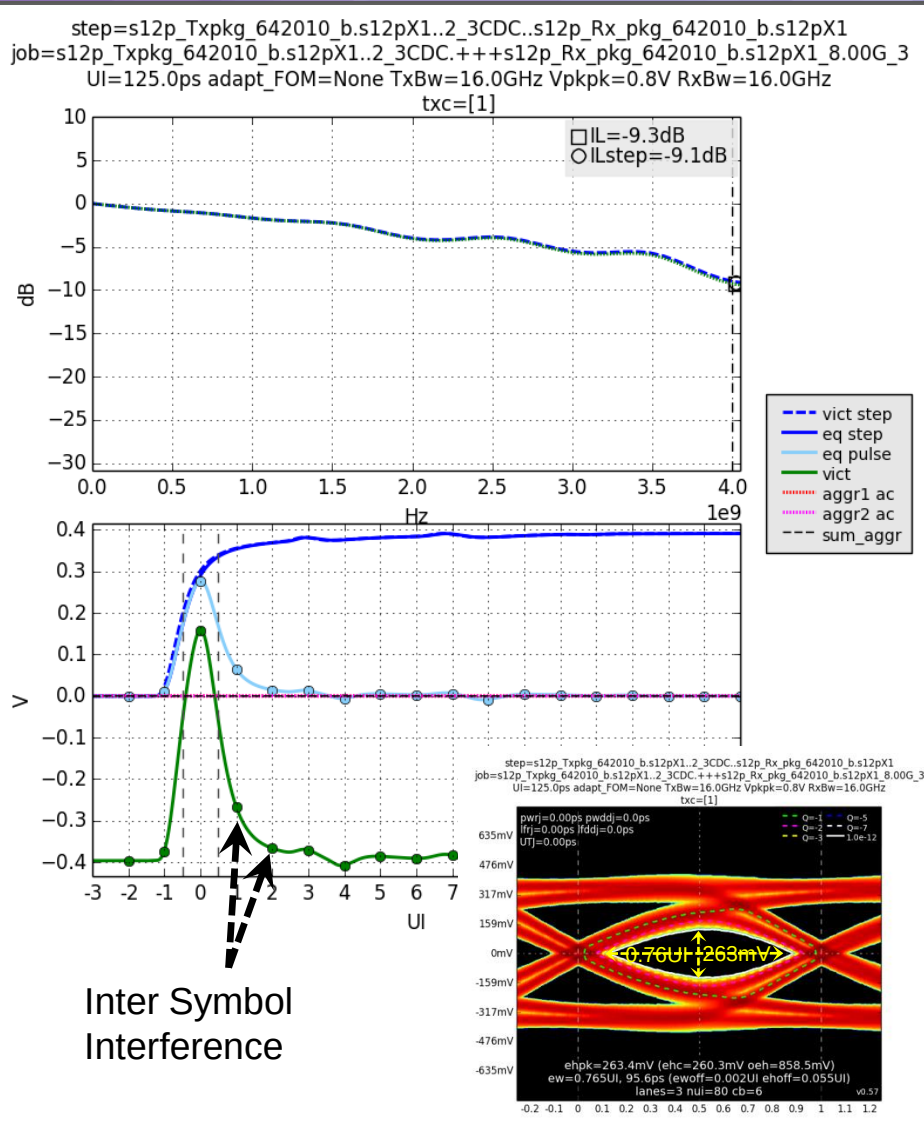
Transmitter circuits use De-Emphasis to equalize the frequency response of the channel in order to minimize inter-symbol interference

Available Equalization Settings:

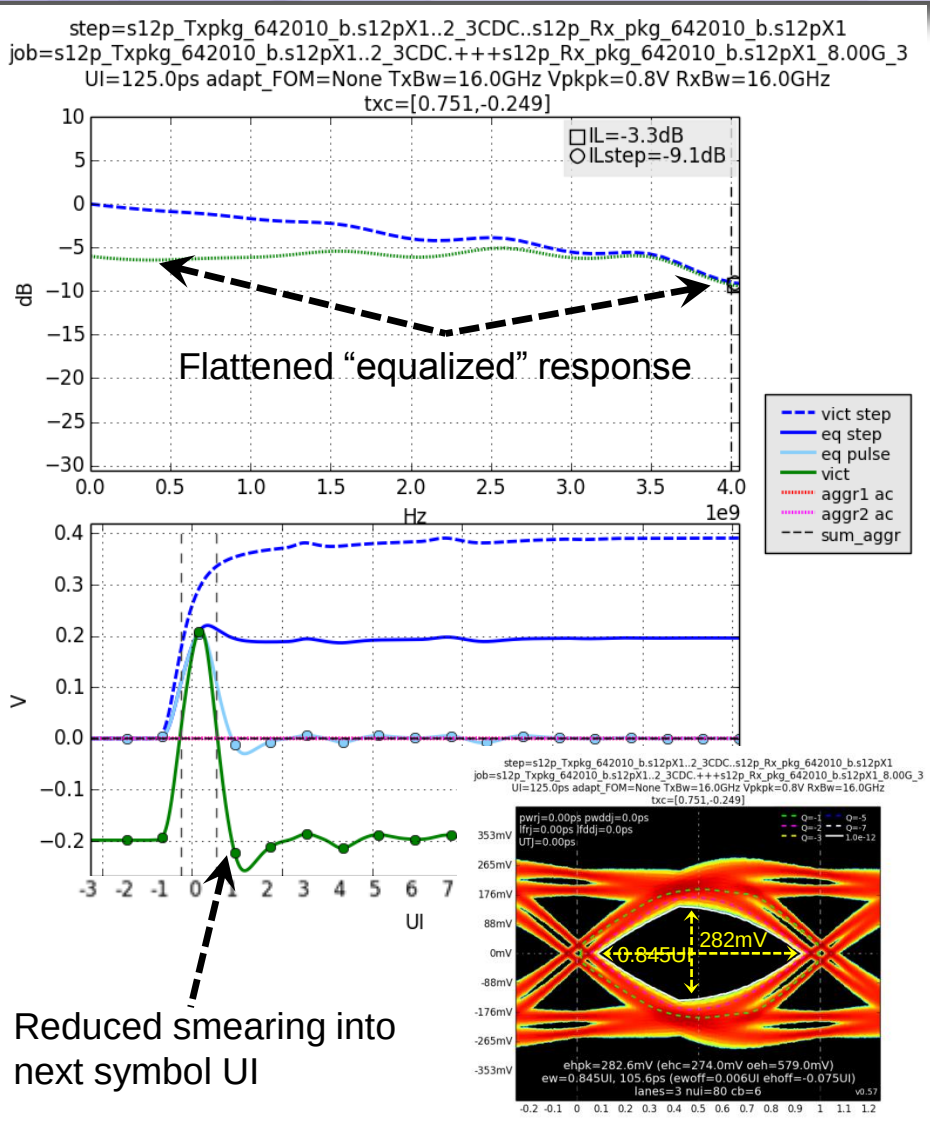
2.5GT/s: [-3.5dB]
5.0GT/s: [-3.5dB, -6dB]
8.0GT/s: [-3.5dB, -6dB, pre-cursor]
* 10-presets
* Coefficient tuning space

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De-Emphasis Pulse & Frequency Domain Response



Inter Symbol Interference

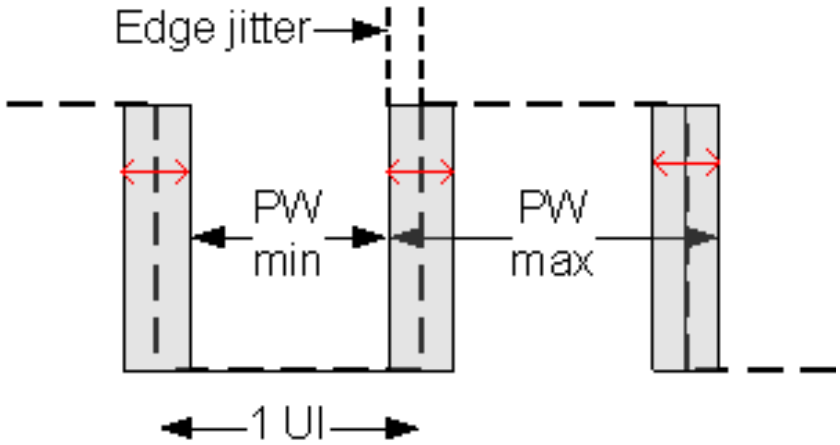


Reduced smearing into next symbol UI

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PCIe Tx Jitter

- **Tx jitter is separated into two categories**
 - Data Dependent: package loss, reflections, ISI
 - Uncorrelated Jitter: PLL jitter, power supply, duty cycle error
- **Pulse Width Jitter (PWJ)**
 - PWJ is a subset of uncorrelated jitter
 - PWJ is amplified by channel loss
 - Edges are assumed to be independent
- **Relationship between pulse width jitter and edge jitter**
 - Important for measurement and channel simulation tools



$PWJ = PW_{max} - PW_{min}$

Edge Jitter DJ= PWJ_DJ/2

Edge Jitter RJ = PWJ_RJ/√2

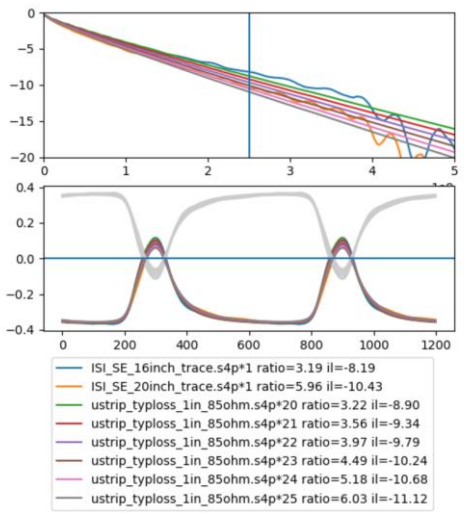
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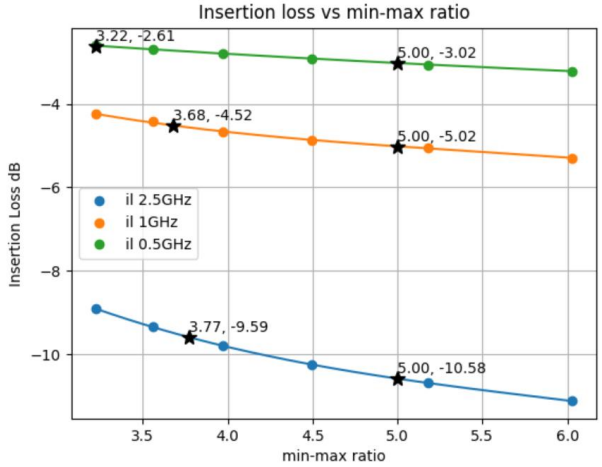
Receiver

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Receiver

- **2.5GT/s and 5GT/s open eye specification, validated at device pin, package included in device budget**
 - Eye height 175/120mV 2.5/5GT/s
 - Eye width 0.4/0.32UI 2.5/5GT/s
 - 2.5GT/s and 5GT/s channel limits





- **8GT/s and 16GT/s closed eye at pin, specified after applying behavioral receiver**
 - Defines minimum Rx EQ performance
 - Used for both Rx stressed eye calibration and channel compliance
 - Eye height 25mV 8GT/s, 15mV 16GT/s
 - Eye width 0.3UI 8GT/s & 16GT/s

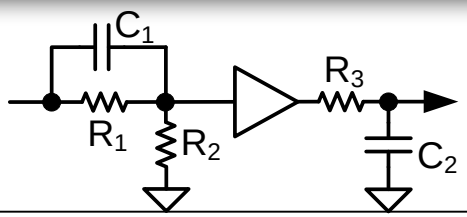
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Receiver Cont.

- **Termination**
 - 100ohm differential
 - 50ohm common-mode
 - 0v common-mode for detect
 - At 8GT/s and 16GT/s Rx allowed to float common-mode
 - Requires LTSSM changes to avoid dead-locks
- **Differential-mode return loss**
 - 10dB 2.5GT/s, 8dB 5GT/s, 5dB 8GT/s
- **Common-mode return loss**
 - 6dB 2.5/5GT/s, 5dB 8GT/s

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Rx Linear Equalizer



$$H(s) = \frac{sC_1R_1R_2 + R_2}{sC_1R_1R_2 + R_1 + R_2} \cdot \frac{1}{sC_2R_3 + 1}$$

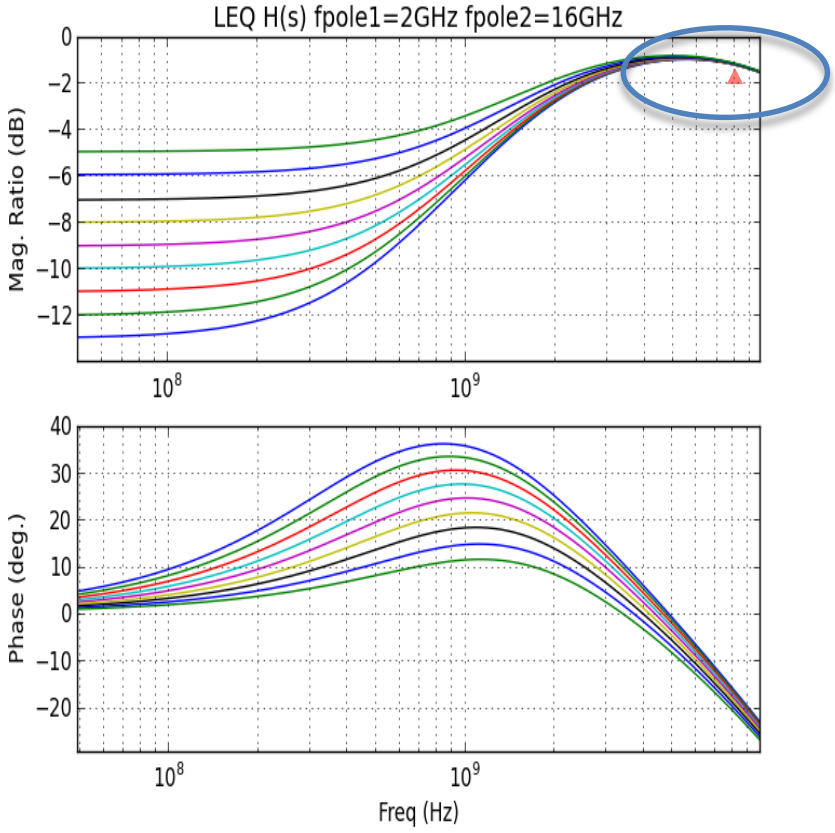
$$H(s) = \frac{R_2}{R_1 + R_2} \cdot \frac{\frac{s}{\omega_Z} + 1}{\frac{s}{\omega_{P1}} + 1} \cdot \frac{1}{\frac{s}{\omega_{P2}} + 1}$$

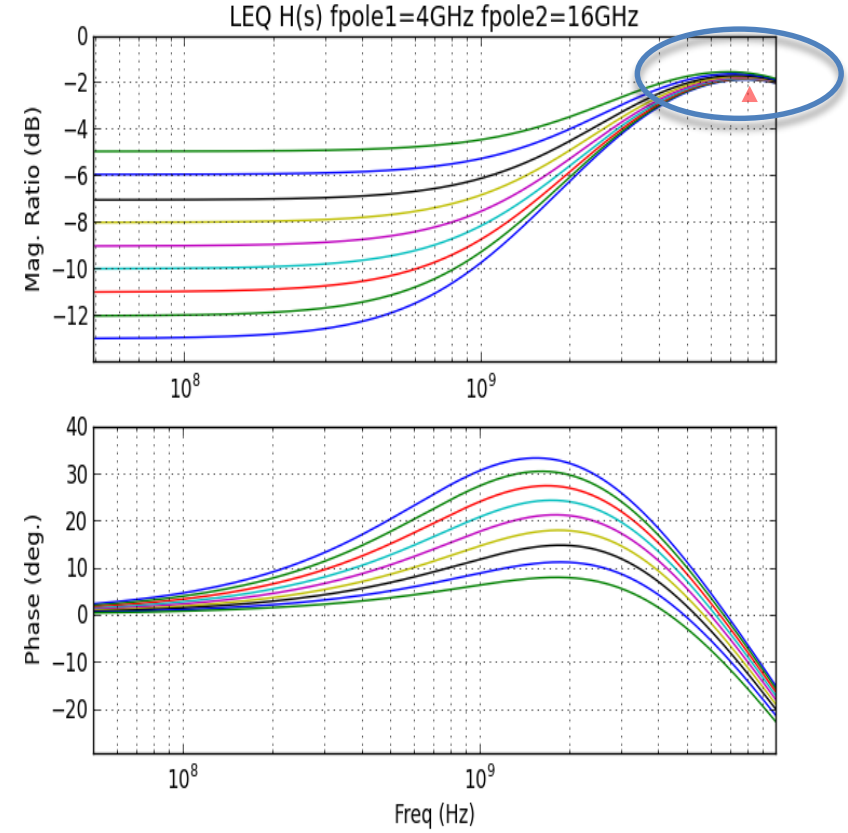
$$G_{DC} = \frac{R_2}{R_1 + R_2}$$

$$\omega_{P1} = \frac{R_1 + R_2}{C_1R_1R_2}$$

$$\omega_Z = \frac{1}{C_1R_1} = G_{DC}\omega_{P1}$$

$$\omega_{P2} = \frac{1}{C_2R_3}$$

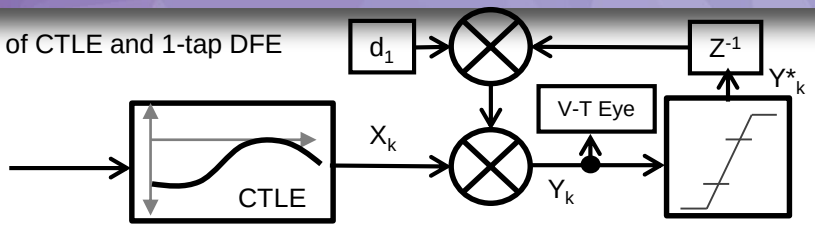




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Behavioral Rx DFE

Block diagram of CTLE and 1-tap DFE

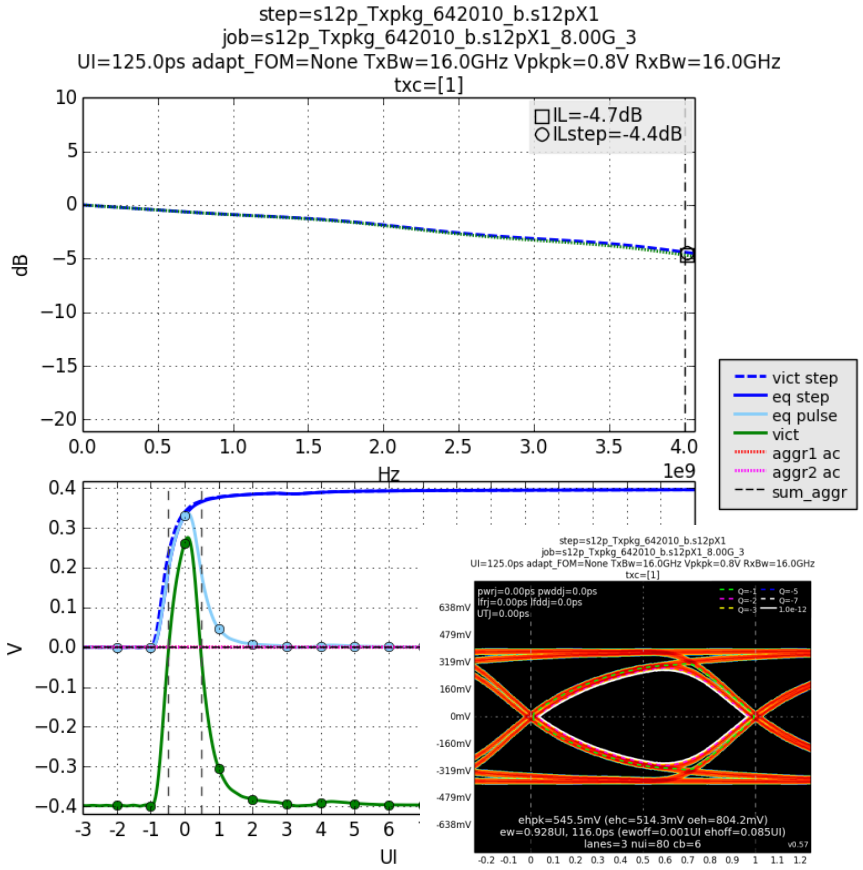


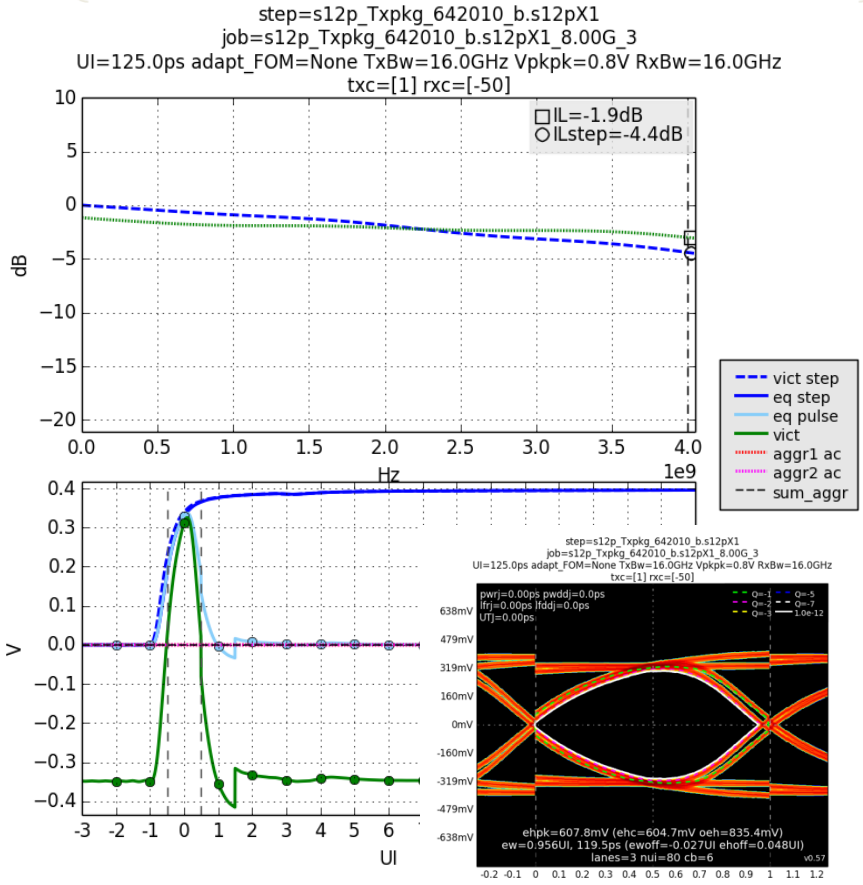
$$Y_k = X_k - d_1 * sgn(Y_k - 1) \Rightarrow DFE\ summer\ Vdiff\ output$$

$Y^*_k \Rightarrow$ *Decision Fn output voltage* $\Rightarrow |Y^*_k| = 1$

$X_k \Rightarrow$ *DFE Vdiff output voltage*

$d_1 \Rightarrow$ *DFE feedback coefficient* K $\Rightarrow$ *sample index*





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Seasim

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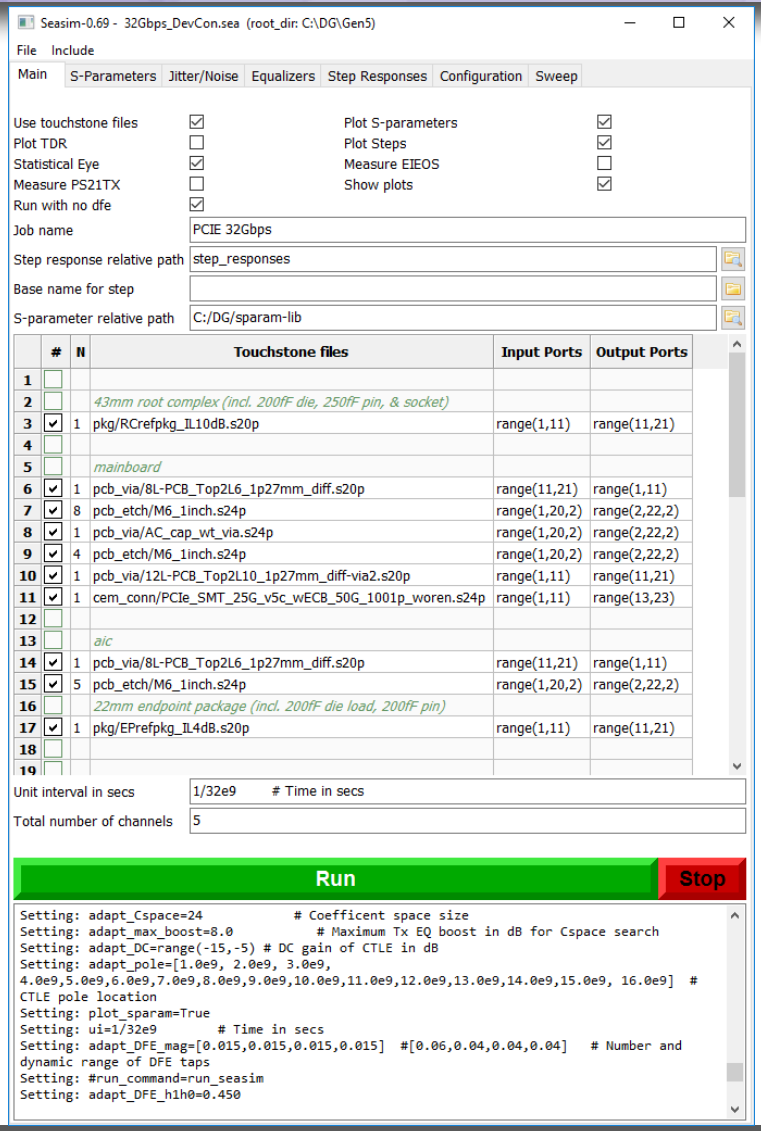
High Speed Channel Simulation Challenges

- **High Frequency response is affected by large number of features in the channel**
 - Pre-layout evaluation of topology choices is a complicated multi-dimensional problem
 - Need to be able to quickly build and test many different options
 - Large number of HVM permutations need to be evaluated to determine robustness of solution
- **Seasim has been developed to allow EWG members to efficiently evaluate these options**

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Seasim Channel Analysis

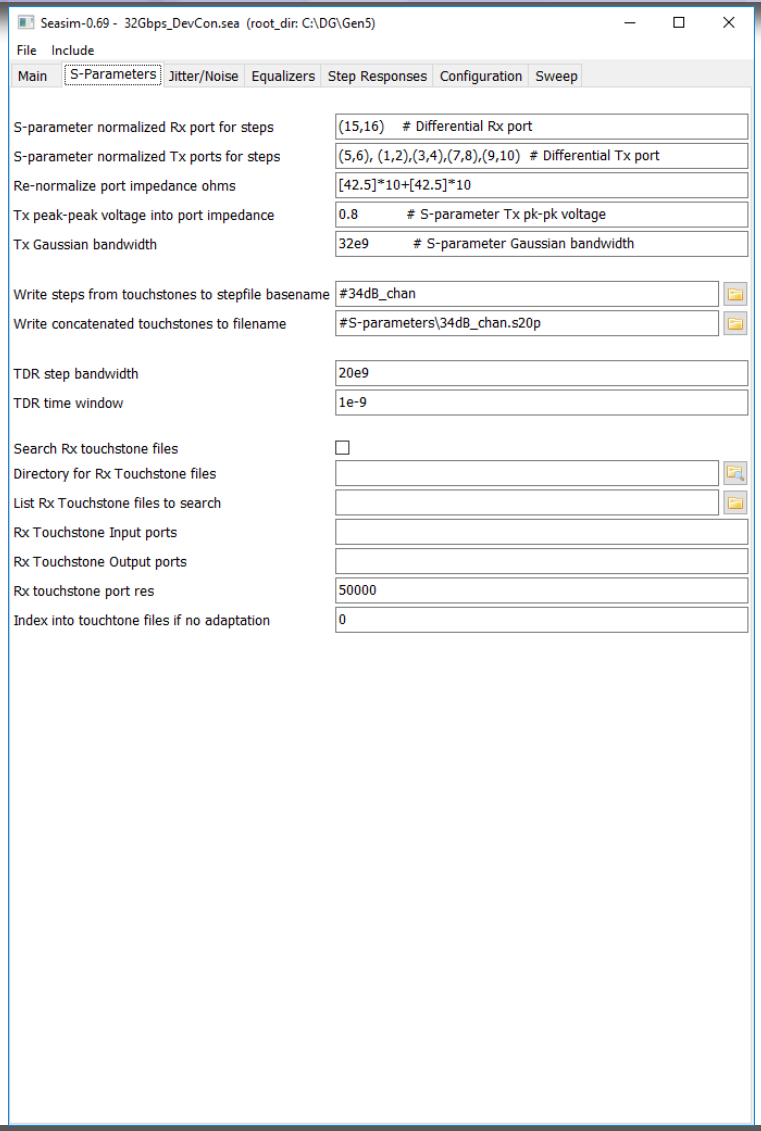
- Allows what-if analysis on the channel components by changing the Touchstone files that are concatenated together for the channel
- Different analyses can be selected as the channel is ‘tuned’
- Either a pre-saved config can be loaded or i.e. pcie-gen4.inc for normal sim conditions
- The other tabs allow simulation conditions to be changed from the default config



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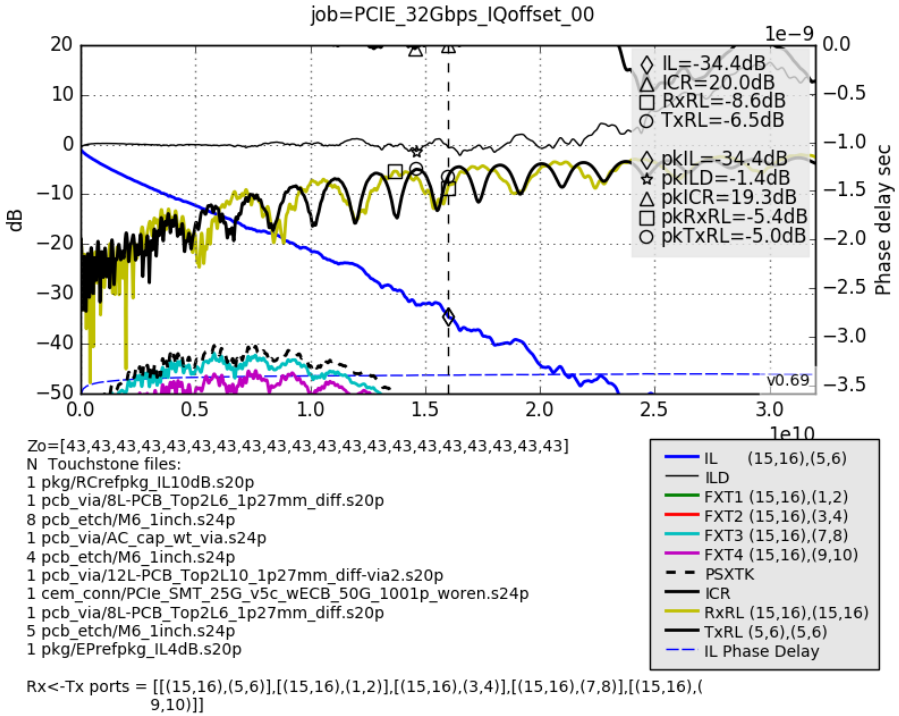
Seasim Port Definitions

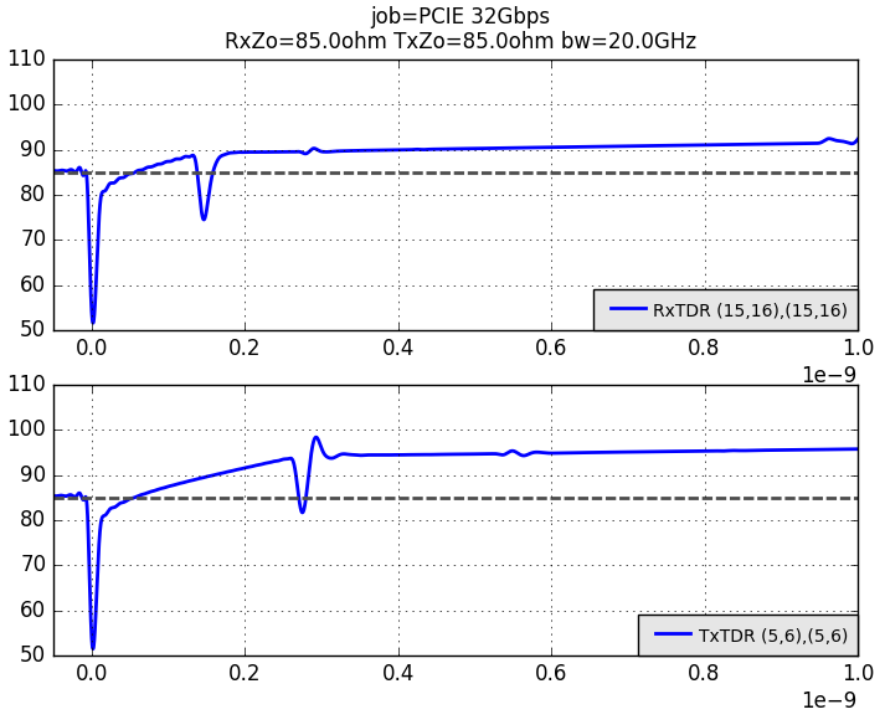
- **Touchstone tuple port definitions**
 - Reflects the S-parameter models intra-pair net order
 - Provides pair-to-pair (victim/aggressor) relationship for crosstalk inclusion
- **Transmitter ports**
 - Allows renormalization of port impedance by providing a list of terminal impedance values
 - Define transmitter pad differential voltage amplitude
 - Transmitter bandwidth defined by Gaussian filter setting
- **Receiver port**
 - Provide custom port renormalization impedance



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Seasim Channel Simulation Frequency Response & Bidir TDR

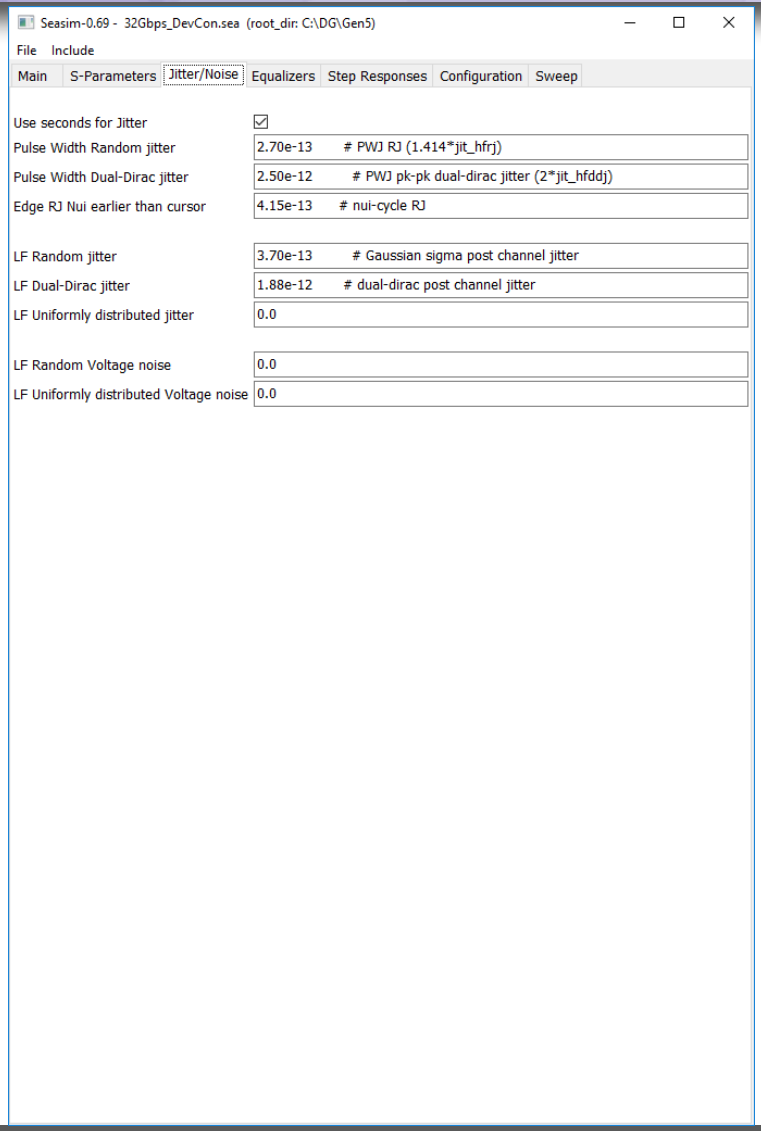




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Seasim Jitter Configuration

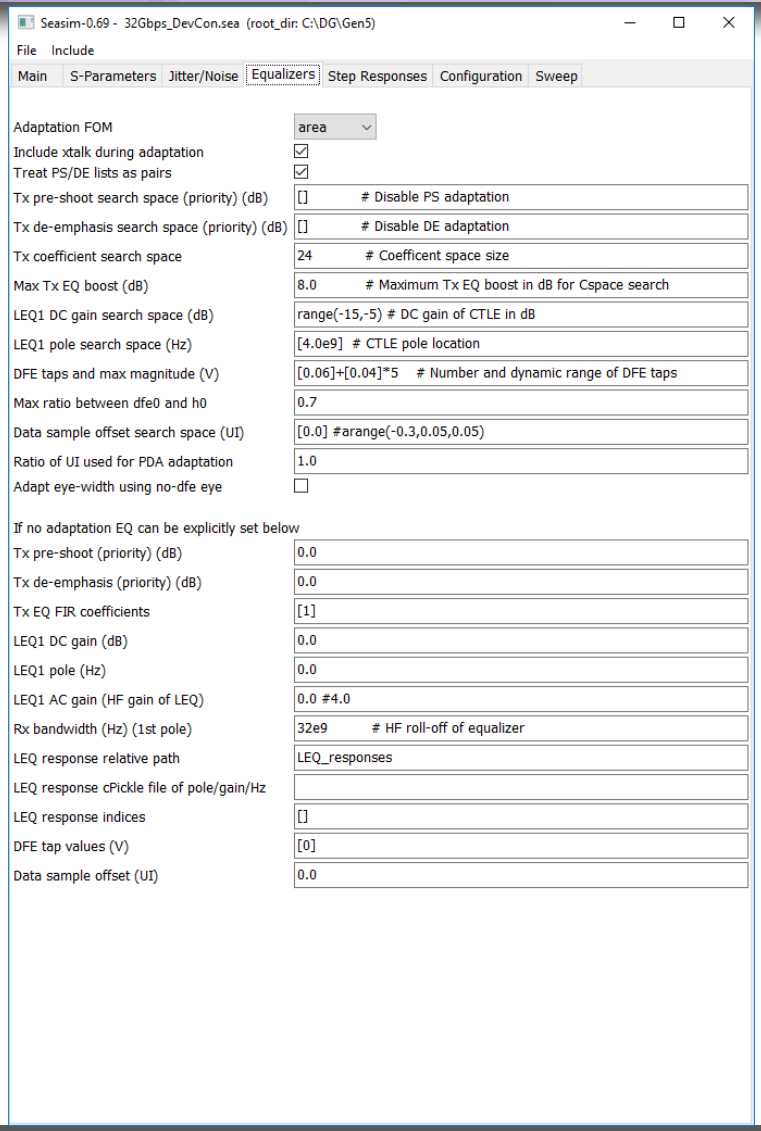
- **Jitter**
 - Consistent jitter definitions with the PCIe base spec
 - Default jitter settings can be loaded with the default configuration file
 - Jitter values can also be customized using the field in the GUI and saved
- **Noise**
 - Random low frequency noise can be defined in addition to the aggressor-victim coupling present in the Touchstone file



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Seasim Equalization

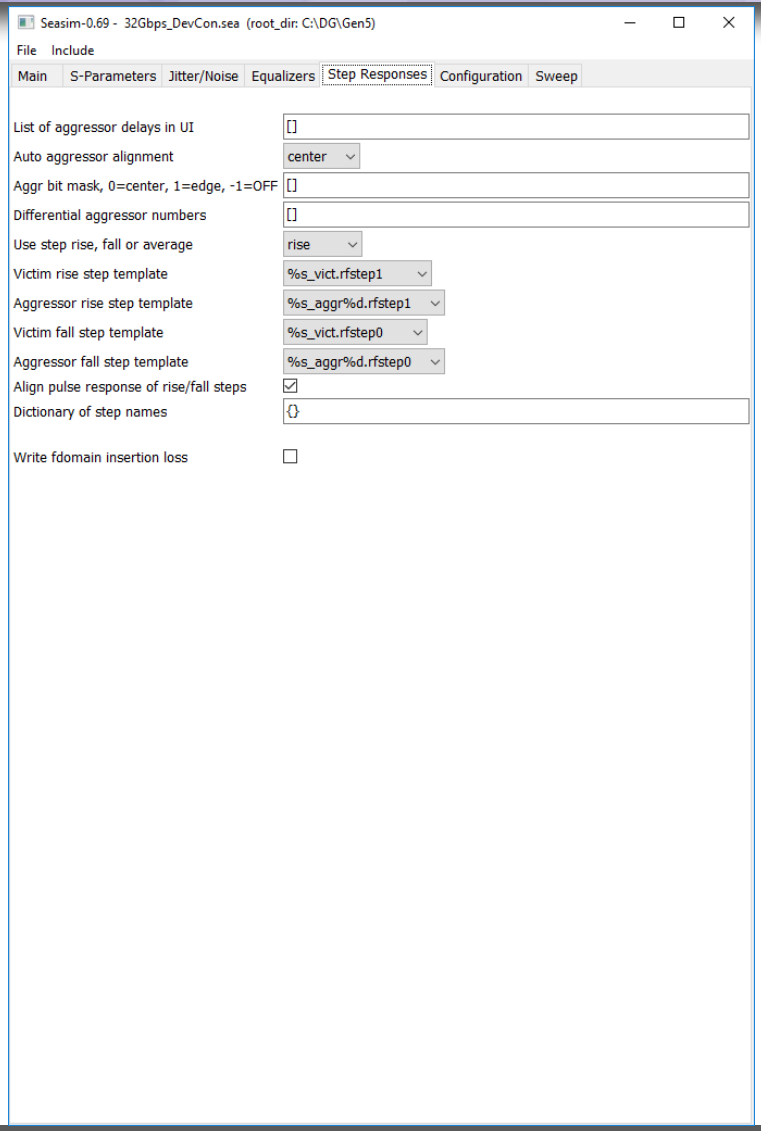
- **Tx FIR Filter**
 - Can either fix pre-shoot and de-emphasis or set coefficient search space for adaptation
- **Rx Linear Equalizer**
 - Define pole/zero value or range of values for adaptation
 - May cascade multiple continuous time LEQ filters
- **Decision Fed Equalizer**
 - Can enable multiple DFE taps beyond defaults
 - Can vary dynamic range of taps independently



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Seasim Step Responses

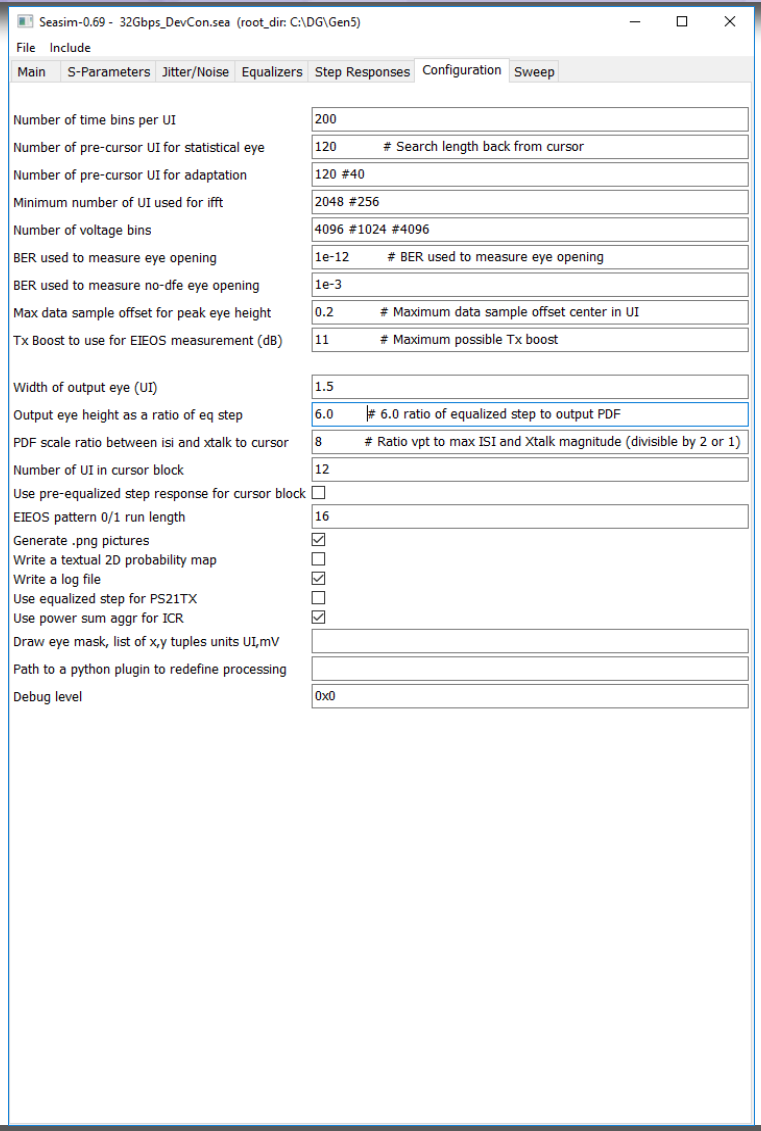
- **Channel Step Response**
 - Alternative simulation method to providing channel S-parameter models
 - Measured or simulated voltage-time records of channel step responses can be used directly for statistical simulation
- **Crosstalk**
 - Independent waveforms can be supplied for the inclusion of aggressor coupling to the victim receiver
 - Can optionally offset the aggressor-to-victim alignment



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Seasim Configuration

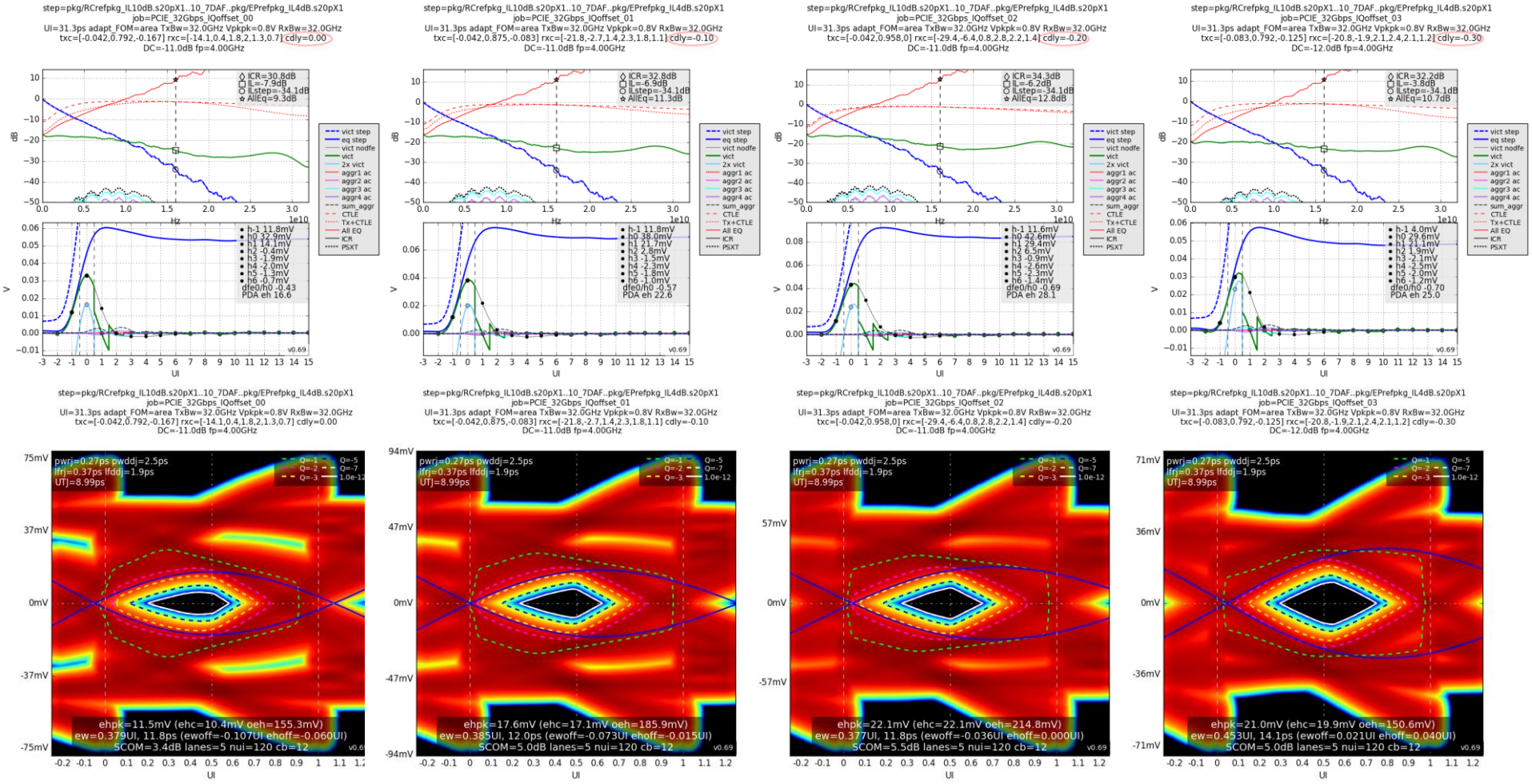
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IQ Offset Adaptation

Left to right increase of data sample-to-edge sample offset, cursor delay (CDLY) token.



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Seasim Sweep

- **Seasim can be used to define HVM sweeps, launch parallel jobs & plot results**
- **The channel model can be swept to represent manufacturing variations of impedance, loss, topology, etc.**
- **Create custom post processing scripts. Use pling to denote custom variable.**

C: > DG > bin > seasim-release-0.69 > extract-sweep-var.py

```
def dfe0(log):
    log.seek(0)
    for line in log:
        if 'rxcoeff' in line:
            name, var = line.split()
            return eval(var)[0]

def postdfe(log, taps=6):
    log.seek(0)
    for line in log:
        if 'h-2_h+16' in line:
            name, var = line.split()
            h = eval(var)
            return sum([abs(x) for x in h[2+taps:2+taps+4]])

def leq_DC(log):
    log.seek(0)
    for line in log:
        if 'leq_DC' in line:
            name, var = line.split()
            return eval(var)

def leq_pole(log):
    log.seek(0)
    for line in log:
        if 'leq_pole' in line:
            name, var = line.split()
            return eval(var)
```



Seasim-0.69 - 32Gbps_DevCon.sea (root_dir: C:\DG\Gen5)

File Include

Main | S-Parameters | Jitter/Noise | Equalizers | Step Responses | Configuration | Sweep

	#	SG	token	IV	
1		1	adapt_DFE_mag	[0.01,0.01,0.01,0.01]	[0.02,0.02,0.
2		2	adapt_DC	range(-28,-5)	range(-21,-5
3		3	adapt_pole	[1.0e9, 2e9, 3e9, 4e9,5e9,6e9,7e9,8e9,9e9,10e9,11e9,12e9]	[1.0e9, 2e9,
4					
5		1	leq_AC	0.0	4.0
6		2	leq_bw	16e9	25e9
7		2	adapt_DFE_mag	[0.06,0.04,0.04,0.04]	[0.06,0.04,0.
8		3	adapt_cursor_delay	[0.0]	[-0.1]
9		3	cursor_delay	0.0	-0.1
10		3	adapt_FOM	area	height
11					
12		1	adapt_cursor_delay	[0.0]	[-0.1]
13		2	port_res	[42.5]*10+[42.5]*10	[42.5]*10+[
14					
15		4	step_portsin	(5,6), (1,2),(3,4),(7,8),(9,10)	(1,2),(3,4),(
16		4	step_portout	(15,16)	(11,12)
17					
18					
19					
20					

Sweep base name: PCIE_32Gbps_IQoffset

Concurrent sims, jobs per sim: 30,1

Run sweep jobs: run_seasim

Kill running jobs

Check job status

List of Sweep Groups for x axis: [1]

Dictionary of "variable":limit: {'!leq_pole':1.0e9, '!leq_DC':-8, 'eh':15,'ew':0.3, '!dfe0':0, '!postdfe':0}

List of anded text filters for y axis: ['height']

Plugin functions for .log parsing: C:\DG\bin\seasim-release-0.69\extract-sweep-var.py

Use sweep text for plot labels ☑

Plot sweep results

Show sweep plots ☑

Delete logs

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